Preliminary Information [1] *(See Last Page)*

FEATURES & APPLICATIONS

- **Two Programmable Reset Outputs, SOFT_RST# And HARD_RST#**
- **De-Bounced Push-Button Reset Input With a Programmable Delay Up To 40 Seconds Prior To Reset Assertion**
- **8 Programmable Settings For Both SOFT_RST# And HARD_RST# Delay**
- **Programmable Voltage Monitor With 8 Voltage Settings To Trigger SOFT_RST# Output**
- **Programmable Reset Output Duration From 1-200ms**
- **Built-In 15us Voltage Glitch Filtering And Input "De-Bouncing"**
- **6 Ball *Ultra* CSP™ (Chip-Scale) Package**
- **8 Lead SOIC Package**

Applications

- **PDAs, Handheld PCs, Cameras, Camcorders**
- **Handheld GPS Equipment**
- **Satellite And Cable-TV Set-Top Box**

INTRODUCTION

The SMR101 is a programmable reset controller especially designed for embedded consumer electronics. The device provides dual outputs that can be used to implement "soft" and "hard" system resets. Both resets can be triggered by an external reset input, and an internal voltage monitor can trigger the soft reset. Typically a "soft" reset applies to volatile registers in an embedded controller while a hard reset is equivalent to a full power cycle without the associated power-up delays. The SMR101 receives an external push-button input using an internal programmable de-bounced timer. The push button input hold down time is programmable up to 40 seconds with an internal on-chip timer. A "short" hold down time (0.125-10 sec) asserts the SOFT_RST# pin while a long hold down time (0.5-40 sec) asserts the HARD_RST# pin. Both reset outputs have programmable output durations from 1-200ms. Additionally, voltage monitoring is provided via a programmable threshold detector (2.30V – 4.50V) on the VDD pin. This voltage detector asserts the SOFT_RST# pin for the same 1-200ms output duration as above. A 15us glitch filter avoids nuisance tripping that can result in unnecessary system resets. The SMR101 is factory programmed, to default values; however, multiplexed programming pins are also provided for in-system programming for prototype purposes.

SIMPLIFIED APPLICATIONS DRAWING

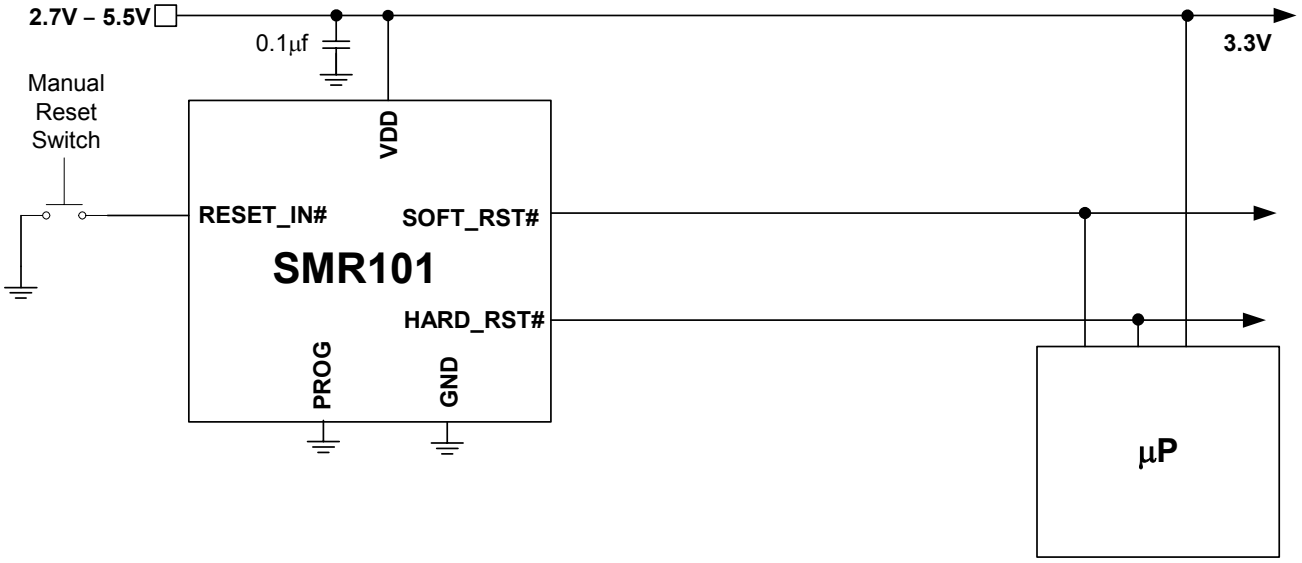


Figure 1 – Applications schematic using the SMR101 to supervise an embedded controller. As shown, the SMR101 implements a two-level RESET function including external manual input.

GENERAL DESCRIPTION

The SMR101 is a programmable reset controller that monitors the power supply in µP and digital systems for under voltage conditions The integrated feature set provides excellent circuit reliability and low cost by eliminating external components while the programmable settings allow “on the fly” adjustments necessary for modern control techniques.

The device performs several functions: it first asserts a “soft” reset signal whenever the VDD supply voltage declines below a preset threshold, keeping it asserted for a programmable time period after VDD has risen above the reset threshold. The part also provides a push button input with two programmable delays for hierarchical manual system reset.

The open-drain SOFT_RST# and HARD_RST# outputs have on-chip 100K pull-up resistors and do not require external pull-up resistors unless more drive current is needed (see figure 3). The SOFT_RST# comparator is designed to ignore fast transients on VDD, and the output is guaranteed to be in the correct logic state for VDD down to 1V. Low supply current makes the SMR101 ideal for use in portable equipment. The RESET_IN# input includes a programmable hold-down delay timer for use with a push button switch for consumer equipment such as set-top boxes and PCs.

A microprocessor’s (µP’s) reset input starts the µP in a known state. The SMR101 asserts a SOFT_RST# to prevent code execution errors during power-up, power-down, or UnderVoltage (UV) conditions whenever the VDD supply voltage declines below a programmed limit (V_{MON}). There are 8 programmable voltage settings to trigger the SOFT_RST# output. SOFT_RST# stays asserted for a programmable period after VDD has risen above the reset threshold. The SOFT_RST# signal is also asserted whenever the RESET_IN# input is asserted for a programmed delay. There are 8 programmable timing settings (T_{RESET_SR}) to trigger SOFT_RST# output. The HARD_RST# signal is also asserted whenever the RESET_IN# input is asserted for a separate programmed delay. There are 8 programmable timing settings (T_{RESET_HR}) to trigger the HARD_RST# output. It is recommended that the soft reset time be of a shorter duration than that of the HARD_RST#.

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the SMR101 is immune to short-duration VDD transients (glitches) due to an internal glitch filter. A external 0.1µF bypass capacitor mounted as close as possible to the VDD pin provides additional transient immunity. Since the SOFT_RST# and HARD_RST# outputs are open drain, the device interfaces easily with µPs that have bidirectional-reset pins. Connecting the SOFT_RST# output directly to the µP’s RESET pin allows either the µP or the SMR101 to assert a reset.

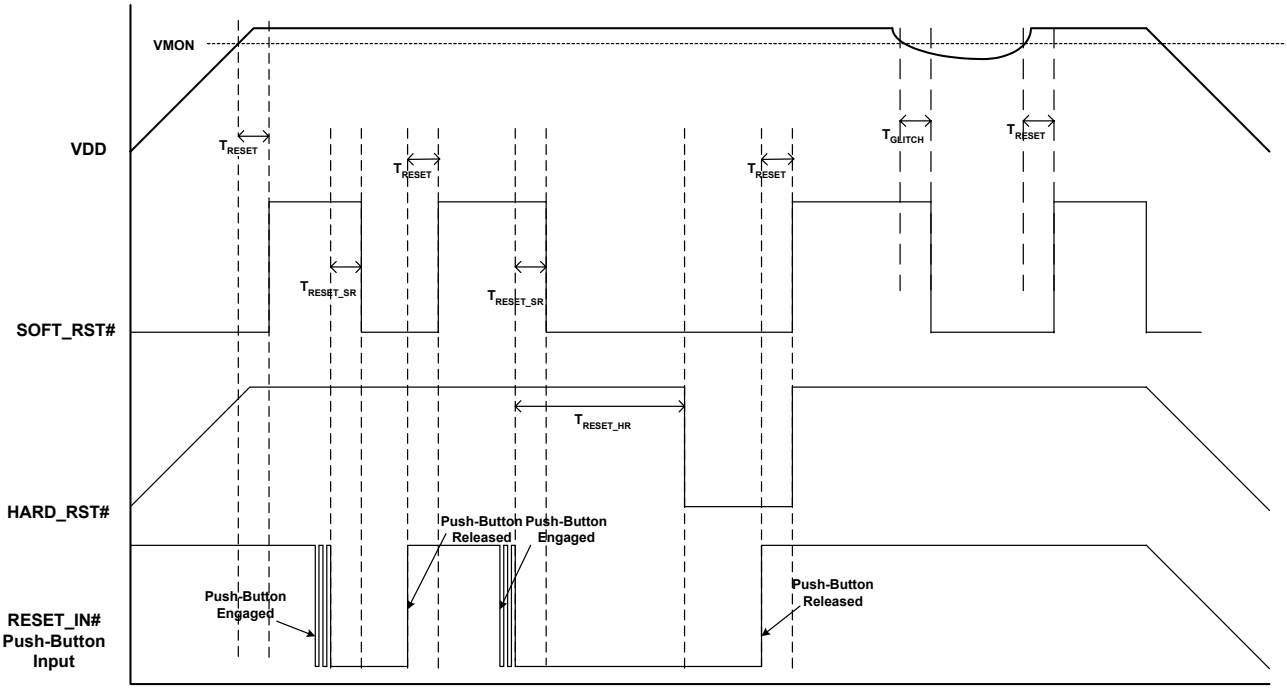


Figure 2 – SMR101 Operation and timing diagram.

INTERNAL BLOCK DIAGRAM

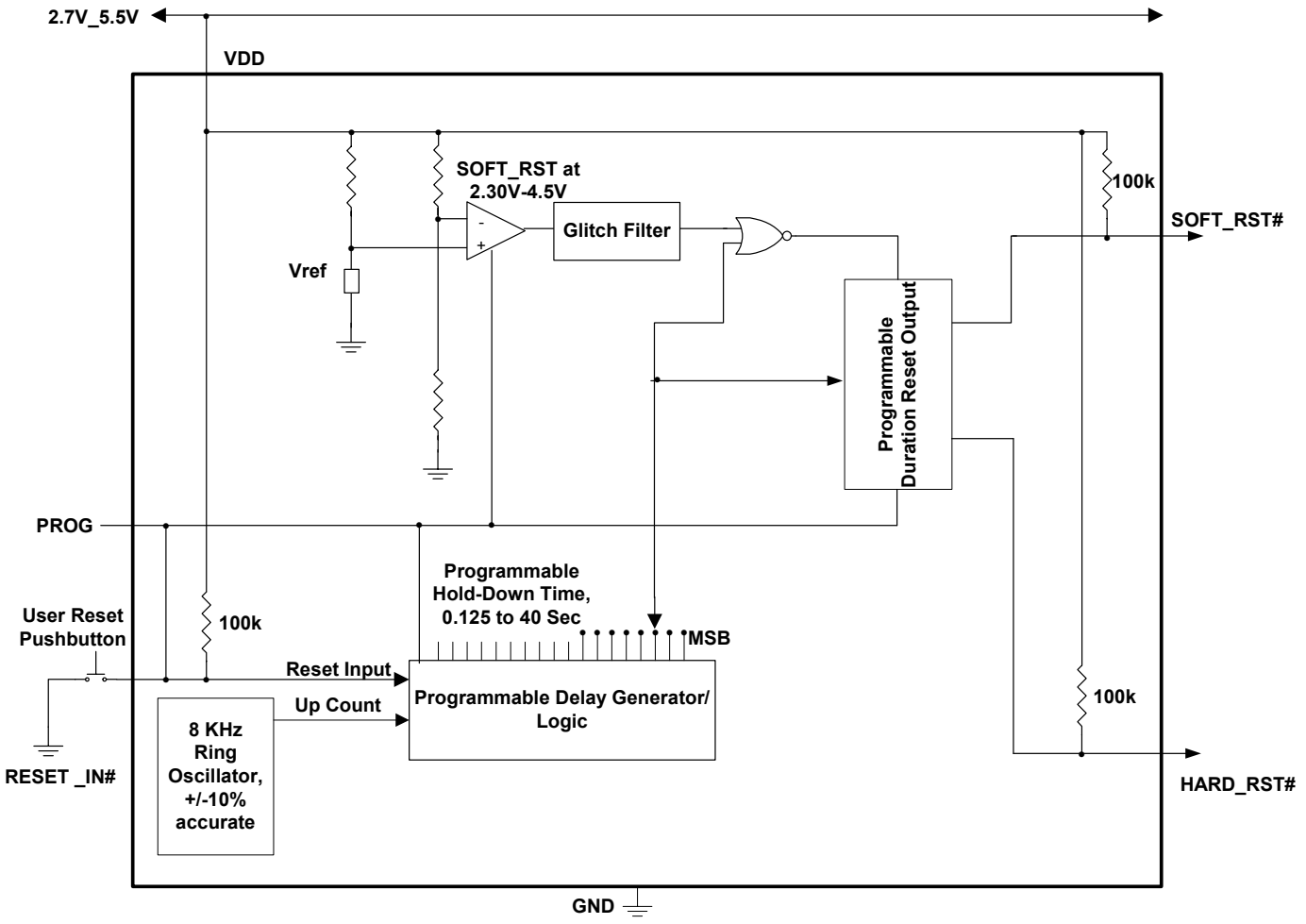


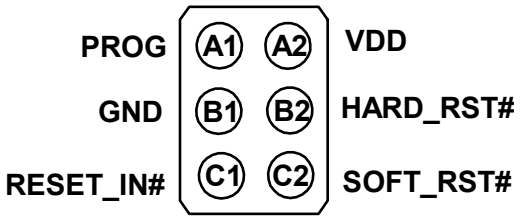
Figure 3 – SMR101 Internal Block Diagram.

Pushbutton Input delay (seconds)				Voltage Monitor Threshold (V)		RESET Timeout Period (ms)	
Register Value	HARD_RST#	Register Value	SOFT_RST#	Register Value	Voltage	Register Value	Time
000	0.5	000	0.125	000	4.50	00	1
001	1	001	0.25	001	4.25	01	25
010	2	010	0.5	010	2.97	10	100
011	4	011	1	011	2.81	11	200
100	8	100	2	100	2.70		
101	16	101	4	101	2.55		
110	32	110	8	110	2.43		
111	40	111	10	111	2.30		

Figure 4 – SMR101 Register Maps. The SMR101 is user programmable using the SMX3199 Programmer and the SMR101 Windows GUI.

PACKAGE AND PIN CONFIGURATION

6 Ball *Ultra* CSP™
Bottom View



8 Lead SOIC
Top View

PIN DESCRIPTIONS

CSP Ball Number	SOIC Lead Number	Pin Type	Pin Name	Pin Description
A1	1	I	**PROG**	High voltage programming pin. Connected to ground during normal operation.
A2	8	PWR	**VDD**	Positive supply voltage.
B1	4	PWR	**GND**	Ground pin.
B2	5	O	**HARD_RST#**	Open Drain active low Hard Reset Out indicator. Internally connected to VDD through a 100KΩ resistor.
C1	3	I	**RESET_IN#**	De-bounced push button switch input. Internally connected to VDD through a 100KΩ resistor. Also used as the Data input programming pin.
C2	6	O	**SOFT_RST#**	Open Drain active low Soft Reset Out indicator. Internally connected to VDD through a 100KΩ resistor.
NA	2,7	NC	**NC**	No Connect

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....-55°C to +125°C

Storage Temperature.....-65°C to +125°C

Terminal Voltage with Respect to GND:

V_{DD} .....-0.3V to +6.0V

PROG, RESET_IN#.....-0.3V to +16.0V

All Others ..... VDD + 0.7V

Output Short Circuit Current 100mA

Reflow Solder Temperature (30 secs).....260°C

ESD Rating per JEDEC.....2000V

Latch-Up testing per JEDEC..... ..... ±100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATION CONDITIONS

Temperature Range (Commercial). .....0°C to +70°C

Supply Voltage[1].....3.3V +/-10%

Note 1 – The device can operate over a supply range of 2.7V to 5.5V.

Package Thermal Resistance (Θ_{JA})

8 Lead SOIC.....23°C/W

6 Ball *Ultra* CSP™ .....TBD°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention.....100 Years

Endurance.....100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
V_{DD}	Supply Voltage Range		2.7	3.3	5.5	V
I_{DD}	Power Supply Current	VDD = 3.3V, no RESET in progress.		40	50	µA
		VDD = 5.5V, no RESET in progress.		55	65	
t_{GLITCH}	Glitch filter time			15	18	µs
V_{IH}	Input High Voltage	VDD = 3.3V	0.9xVDD		VDD	V
V_{IL}	Input Low Voltage	VDD = 3.3V			0.1xVDD	V
V_{OL}	Open Drain Outputs (HARD_RST#, SOFT_RST#)	ISINK = 1mA	0		0.4	V
I_{OL}	Output Low Current		0		1.0	mA

AC OPERATING CHARACTERISTICS

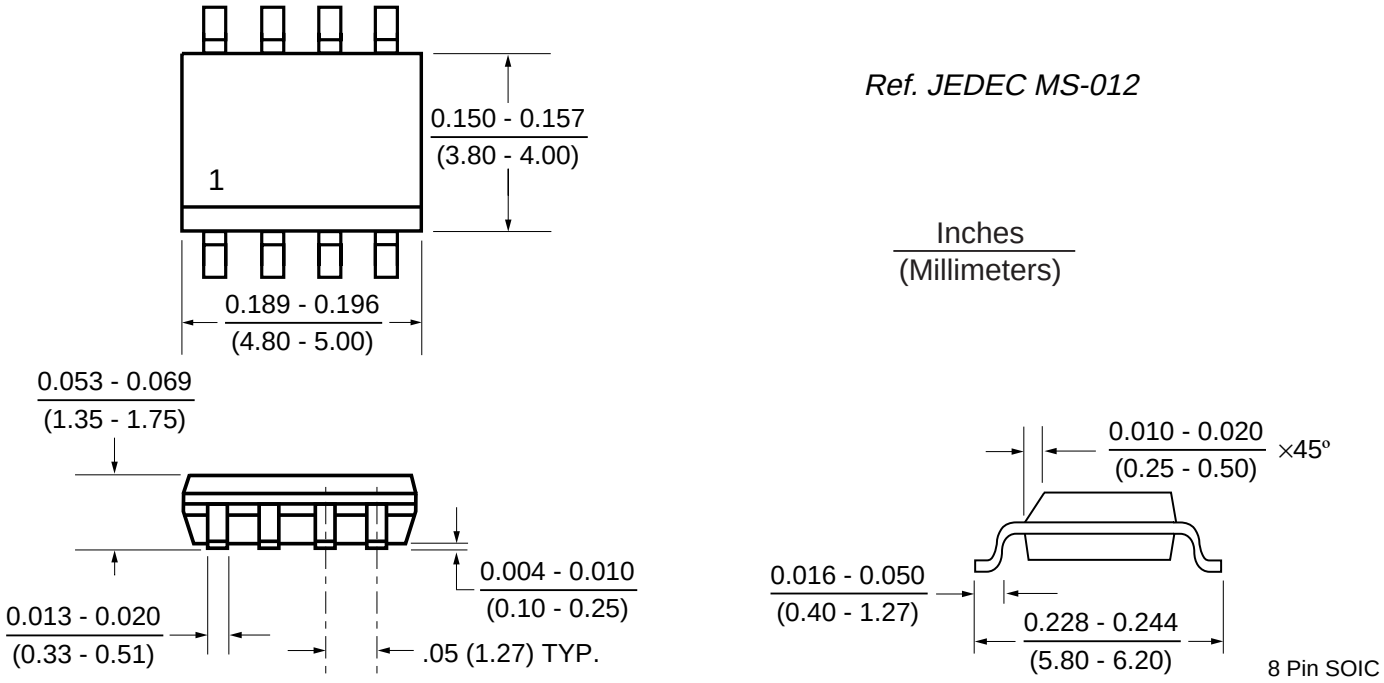
(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
T_{RESET}	Reset Output Timeout period	Programmed Default = 100ms	0.80	1	1.20	ms
			20	25	30	ms
			80	100	120	ms
			160	200	240	ms
V_{MON}	Voltage Monitor Threshold[1]	Programmed Default = 2.97V	4.41	4.5	4.59	V
			4.16	4.25	4.34	V
			2.91	2.97	3.03	V
			2.75	2.81	2.87	V
			2.64	2.7	2.76	V
			2.5	2.55	2.6	V
			2.38	2.43	2.48	V
			2.25	2.3	2.35	V
T_{RESET_SR}	Programmable Reset Hold-Down Delay times (soft reset)	Programmed Default = 0.25s	0.10	0.125	0.15	s
			0.20	0.25	0.30	s
			0.40	0.5	0.60	s
			0.80	1	1.20	s
			1.60	2	2.40	s
			3.20	4	4.80	s
			6.40	8	9.60	s
			8	10	12	s
T_{RESET_HR}	Programmable Reset Hold-Down Delay times (hard reset)	Programmed Default = 4s	0.40	0.5	0.60	s
			0.80	1	1.20	s
			1.60	2	2.40	s
			3.20	4	4.80	s
			6.40	8	9.60	s
			12.80	16	19.20	s
			25.60	32	38.40	s
			32	40	48	s

Note 1 - Voltage monitor threshold accuracies are relative to factory programmed setting, deviation from this setting can result in errors exceeding those stated above.

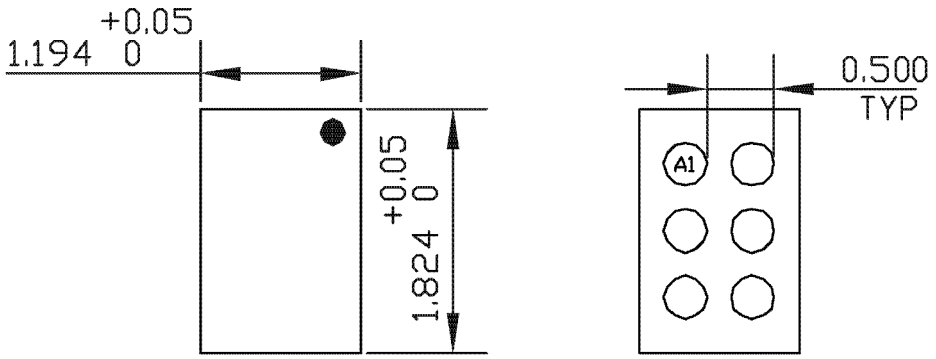
PACKAGE OUTLINE

8 Lead SOIC Package

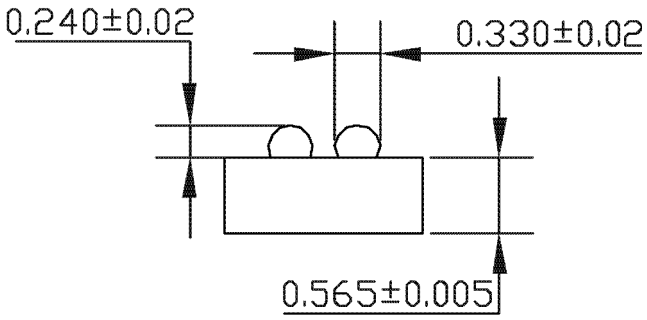


PACKAGE OUTLINE (CONTINUED)

6 Ball *Ultra* CSP™ – Chip Scale Package



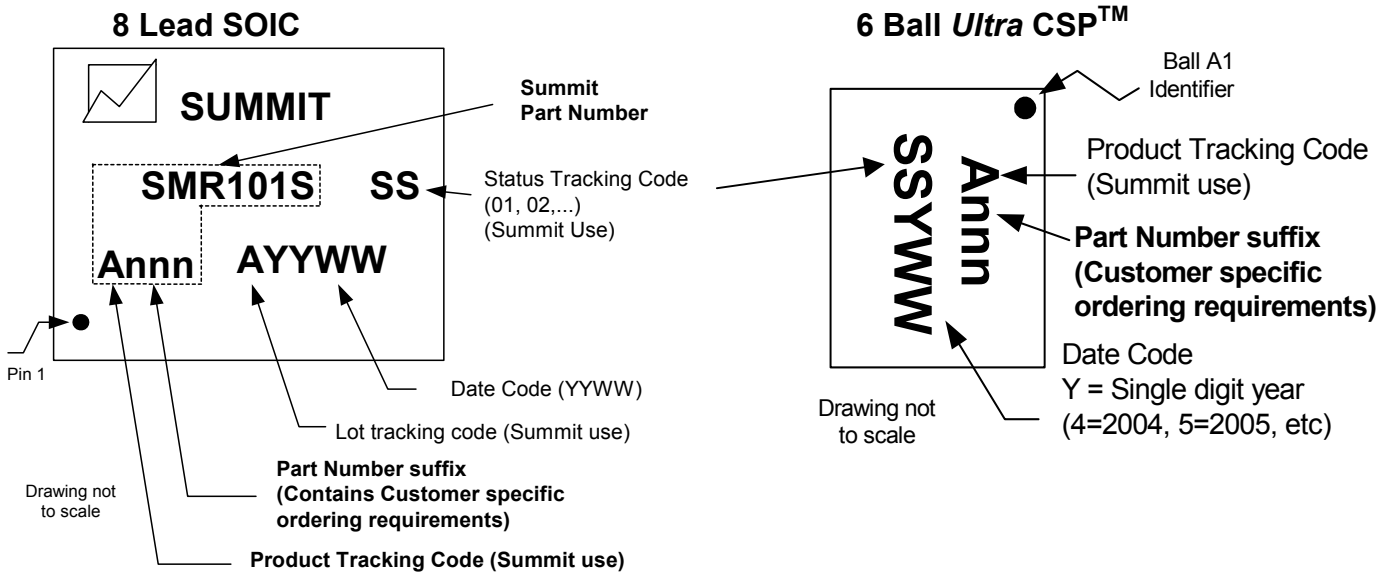
TOP VIEW BOTTOM VIEW



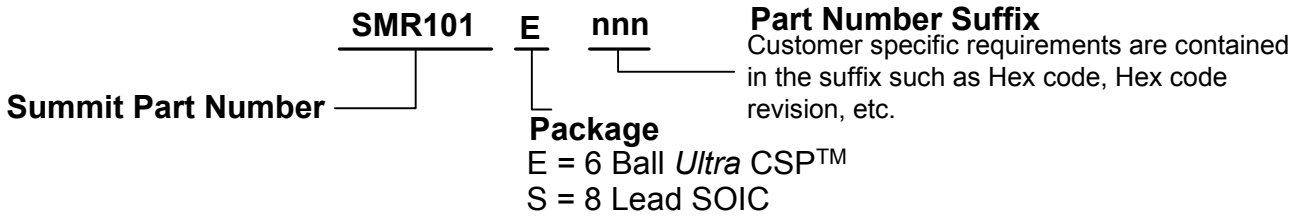
SIDE VIEW

NOTES:
1. SOLDER COMPOSITION IS Sn 63% , Pb 37%
2. MELTING POINT IS 182°C ± 2°C
3. PART IS LASER MARKED 0.3mm FONT HEIGHT.
   0.2mm FONT PITCH.
   WHITE MARKING
   DEPTH: 3 TO 8um
4. ALL DIMENSIONS ARE IN MILLIMETERS [mm]

PART MARKING



ORDERING INFORMATION



The default device ordering number is SMR101E-316 and is programmed as described in the AC Operating Characteristics table on page 6 and tested over the commercial temperature range.

NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

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Device Errata sheets can be accessed at: http://www.summitmicro.com/errata/

Revision 2.1 - This document supersedes all previous versions. Please check the Summit Microelectronics Inc. web site at http://www.summitmicro.com for data sheet updates.

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